## REMARKS

Claims 1 and 3-9 are pending.

Claim 1 has been amended to incorporate the features of claim 2 (now canceled).

In the Office action, claims 1-9 were rejected as follows:

* Claims 1-4 and 7 were rejected as anticipated by U.S. Application No. 2004/0151449 (Nakagawa et al.).

* Claim 5 was rejected was unpatentable over the Nakagawa et al. application in view of U.S. Patent No. 4,418,332 (Mefford).

* Claims 8-9 were rejected as unpatentable over the Nakagawa et al. application.

Nakagawa et al.

FIG. 10 of the of the Nakagawa et al. application discloses charge transfer transistors (Q1-Qn) and capacitors (C1-Cn). One end of each capacitor is coupled to the charge transfer transistors. Clock pulses (CLK1, CLK2) are provided to the other end of each capacitor based on a clock signal (clk) and a startup time control signal (Scon) passed through buffers (B11, B21) to drive the clock signals.

Details of the buffers (B11, B21) according to one implementation are illustrated in FIG. 11 and described starting at par. [0132]. The signals 'clk' and 'Scon' control the transistors Q21 through Q26. During an initial time period, the amplitudes of the clock signals (CLK1, CLK2) are at a reduced level (see FIG. 12(a)). After a predetermined period ($\tau$) elapses, the amplitude is increased to Vdd (see FIG. 12(b)).

In particular, as explained in pars. [0133] through [0138], initially the signal Scon remains low and, therefore, the transistors Q21 and Q24 are OFF. That results in a voltage drop across transistors Q25 and Q26 so that the clock signals (e.g., CLK1) are at the reduced level as shown in FIG. 12(a). After the predetermined period ($\tau$), the signal Scon goes HIGH so that Q21-Q24 are turned ON. That removes the voltage drop across Q25 and Q26 so that the clock signals (e.g., CLK1) are at the higher amplitude as shown in FIG. 12(b).

The claims are patentable over the Nakagawa et al. application

Claim 1 recites a charge pump circuit with first and second clock drivers for supplying clock pulses to an end of a capacitor. He charge pump circuit includes a clock driver control circuit for initiating operation of the first clock driver when the charge pump circuit starts operating and initiating operation of the second clock driver after a predetermined elapsed time. The clock driver control circuit stops operation of the first clock driver at an end of the predetermined elapsed time

Even if, as alleged by the Office action, the transistors Q21-Q26 in the buffer B11 of the Nakagawa et al. application were considered to correspond to the first and second clock drivers recited in claim 1, the operation of the first clock driver is not "stopped" as recited in that claim.

According to the Nakagawa et al. application, all that occurs after the predetermined period ($\tau$) elapses is that the transistors Q21-Q24 are turned ON. That does not "stop" the operation of the transistors Q25-Q26, but (as explained above) simply removes the voltage drop across those transistors.

At least for those reasons, claim 1, as well as dependent claims 3-7, should be allowed.

Furthermore, dependent claims 3-7 include additional features that make those claims independently patentable. For example, claim 3 recites a control circuit to control the first and second clock drivers according to an output signal of a comparator. Similarly, claim 7 recites a control circuit to control the first and second clock drivers according to an output signal of a counter.

The Office action alleges that the inverter circuit (NOT3) corresponds to the "control circuit" of claims 3 and 7. That is incorrect. Although the inverter circuit (NOT3) may receive a signal (Scon) from a comparator (FIG. 15) or timer that counts (FIG. 10), the inverter circuit (NOT3) does not control both the first and second clock drivers in FIG. 11. In particular, the Office action alleges (page 2, par. 2) that the transistors Q25, Q22, Q23 and Q26 collectively correspond to the "first clock driver" and that the transistors Q21-Q24 collectively correspond to the "second clock driver." However, as is evident from FIG. 11, the inverter circuit (NOT3)

does not control the transistors Q25, Q22, Q23 and Q26, which allegedly correspond to the "first clock driver." Therefore, there is no disclosure or suggestion of "a control circuit which controls the first clock driver and the second clock driver" as recited in claims 3 and 7.

Claims 3-7 should be allowed for those additional reasons as well.

Moreover, the additional feature of claim 4 (that the predetermined reference voltage is equal to a power supply voltage) also is not disclosed by the Nakagawa et al. application.

FIG. 15 of the Nakagawa et al. application discloses an implementation in which the signal Scon is provided as the output from an operational amplifier (OP1). The op amp (OP1) compares a reference signal (Vref) to a signal (Vs) that is based on the output voltage (Vout) of the charge pump circuit. The voltage Vs is obtained by dividing the output voltage Vout using resistors R3, R4.

In contrast to pending claim 4, the reference voltage (Vref) in the Nakagawa et al. application is not "equal to" the power supply voltage (Vdd) because of the resistors R5, R6.

For that additional reason, claim 4 should be allowed.

The Mefford patent does not disclose or suggest the claimed features missing from the Nakagawa et al. application.

The Office action alleges that independent claim 8 would have been obvious from the Nakagawa et al. application by simply duplicating the charge pump circuit of FIG. 10. Applicant respectfully disagrees.

Claim 8 recites a clock driver control circuit for initiating at least four clock drivers in a particular sequence and with respect to particular timing. In particular, both the third and fourth clock drivers (which are part of the second charge pump circuit) are initiated after the first and second clock drivers (which are part of the first charge pump circuit). There is no suggestion in the Nakagawa et al. application of a clock driver control circuit for initiating two charge pump

circuits in that way. Therefore, the statement in the Office action (at page 4, par. 5) fails to address that feature and the subject matter of claim 8 as a whole.

At least for those reasons, claims 8 and 9 should be allowed as well.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Please apply other charges or credits to deposit account 06-1050.

Respectfully submitted,

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